

### DESCRIPTION

The GLF4010 and GLF4012 are ultra-low I<sub>Q</sub> integrated power multiplexer IC with dual independent power switches connected to a single output pin to enable seamless transition between two input sources. The GLF4010 and GLF4012 feature symmetrical power FET characteristics. Channel 1 (VIN1) and channel 2 (VIN2) provide ultra-low conduction resistance to support 6 A continuous current capability. It is an ideal solution for a power system with an internal back up power source.

The GLF4010 and GLF4012 provide an automatic selection mode, a manual selection mode and VIN1 preference mode. The switching of these three modes is executed by combining the S1 and S2 pin settings. The S1 input pin has an internal threshold voltage to offer a preference to select the channel 1 (VIN1) power source. In the automatic input selection mode, the GLF4010 and GLF4012 automatically select a higher input voltage source between two input power sources.

The GLF4010 and GLF4012 prevent cross conduction current between two input sources. When VOUT is higher than VIN, the GLF4012 prevents the reverse current from the output to the input, no matter which input supply is applied.

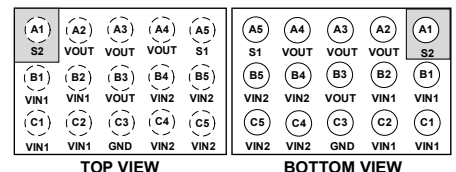
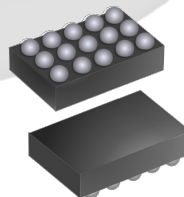
### FEATURES

- Two-Input and Single-Output Power Multiplexer IC
- Auto & Manual & VIN1 Preference Selection Mode
- Wide Input Range: 1.5 V to 5.5 V
- Low R<sub>ON</sub>
  - 15 mΩ Typ at 5.5 V<sub>IN</sub>
- I<sub>OUT</sub> Max: 6 A Per Channel, VIN1 and VIN2
- Ultra-low Quiescent Current
  - I<sub>Q</sub> : 1.4 μA Typ at 5.5 V<sub>IN</sub>
- Low Shutdown Current
  - I<sub>SD</sub> : 1.0 μA Typ at 5.5 V<sub>IN</sub>
- Reverse Current Blocking Protection: Only GLF4012
- Thermal Shutdown Protection
- Wide Operating Temperature Range: - 40 °C to 105 °C

### APPLICATIONS

- Smart Door Lock
- Subsystem with Backup Power
- Multi-channel Power Management
- Communication / Network System

### PACKAGE



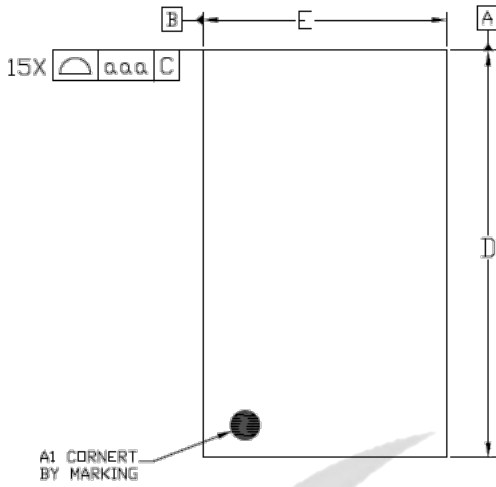
**1.17 mm x 1.97 mm x 0.55 mm WLCSP**

**PRODUCT INFORMATION**

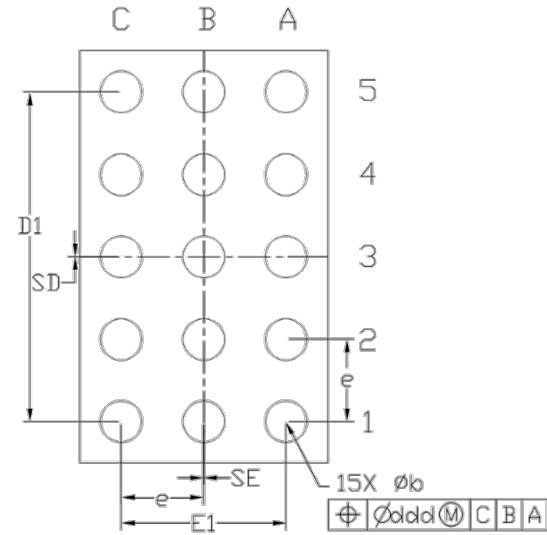
Part Number	Top Mark	R <sub>ON</sub> (Typ.)	I <sub>OUT</sub> (Max)	Reverse Current Blocking	Output Discharge (Typ.)	Package	DS Status
GLF4010-SA7	IA	15 mΩ	6 A	NA	NA	1.17 mm x 1.97 mm x 0.55 mm WLCSP	Preliminary
GLF4011-SA7	IB			YES	100 Ω		On Request
GLF4012-SA7	IC			YES	NA		Product



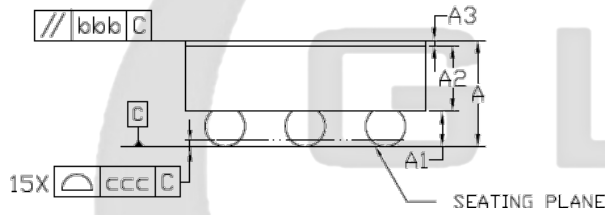
**PACKAGE OUTLINE**



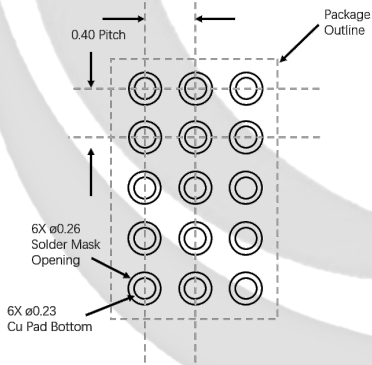
**TOP VIEW**



**BOTTOM VIEW**



**Recommended Footprint**



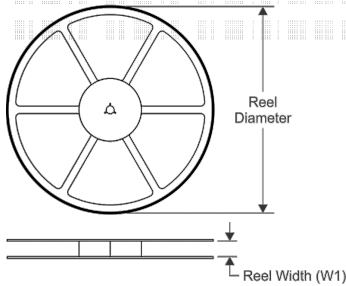
REF.	Dimensions Ref.		
	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.149	0.175	0.201
A2	0.325	0.350	0.375
A3	0.020	0.025	0.030
D	1.955	1.970	1.985
E	1.155	1.170	1.185
D1	1.550	1.600	1.650
E1	0.750	0.800	0.850
b	0.197	0.232	0.267
e	0.400 BSC		
SD	0.000 BSC		
SE	0.000 BSC		
Tol. of Form & Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

**Notes**

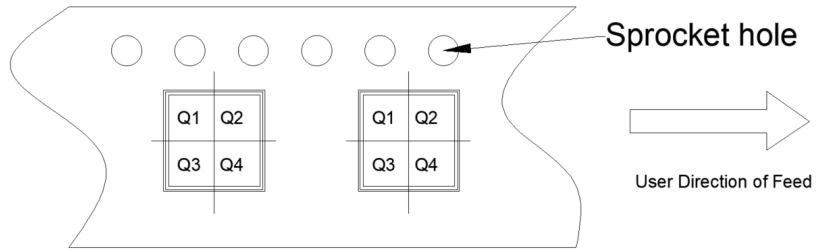
1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

**TAPE AND REEL INFORMATION**

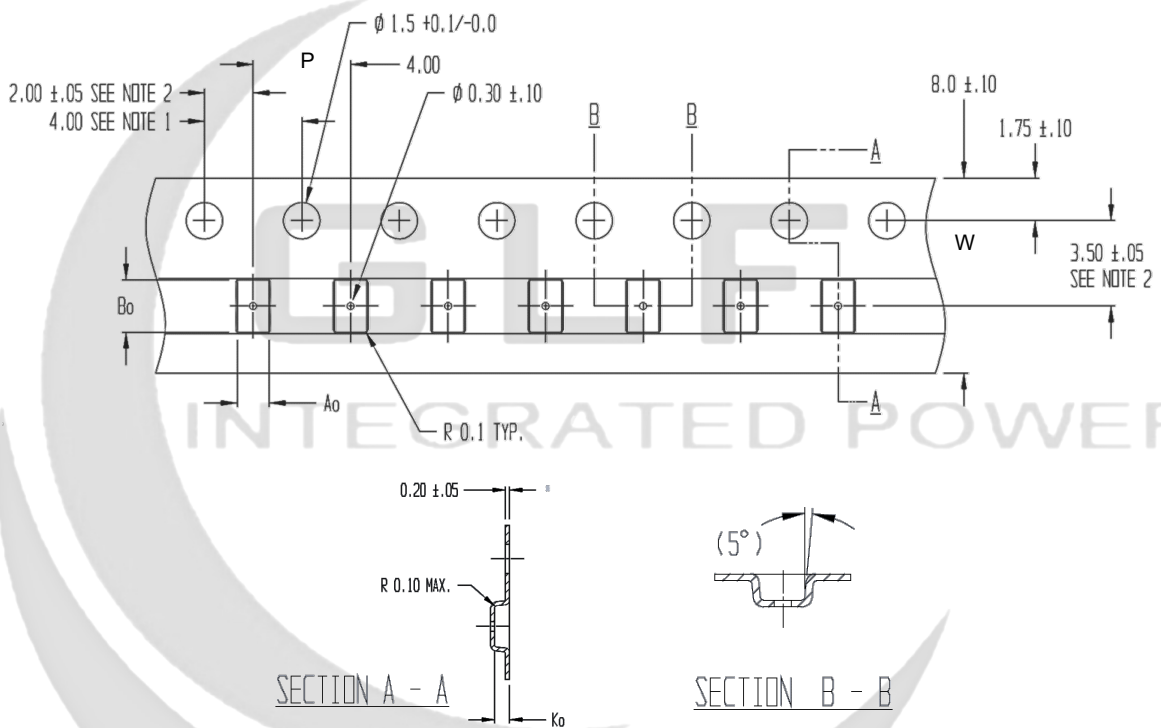
**REEL DIMENSIONS**



**QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE**



**TAPE DIMENSIONS**



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF4010-SA7	WLCSP	15	3000	180	9	1.32	2.15	0.77	4	8	Q2
GLF4012-SA7	WLCSP	15	3000	180	9	1.32	2.15	0.77	4	8	Q2

**Remark:**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P: Pitch between successive cavity centers